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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,682	07/31/2006	Katsumi Shibayama	46884-5426	8343
55694 7590 06/01/2007 DRINKER BIDDLE & REATH (DC) 1500 K STREET, N.W. SUITE 1100 WASHINGTON, DC 20005-1209			EXAMINER PATEL, REEMA	
			ART UNIT 2812	PAPER NUMBER
			MAIL DATE 06/01/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/550,682

**Applicant(s)**

SHIBAYAMA, KATSUMI

**Examiner**

Reema Patel

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/31/06, 9/26/06, 1/18/07, 5/7/07</u> .                       | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The information disclosure statements (IDS) were submitted on 7/31/06, 9/26/06, 1/18/07, and 5/7/07. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

### ***Drawings***

3. Figure 26 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3-6, and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneta et al. (2003/0034496 A1) in view of Akahori et al. (2001/0045577 A1).

6. Regarding claim 1, Yoneta et al. discloses a photodiode array comprising a semiconductor substrate, wherein a plurality of photodiodes are formed in an array on an opposite surface side to an incident surface of light to be detected ([0038]-[0039]). Yet, Yoneta et al. does not disclose providing a resin film that covers regions corresponding to regions where the photodiodes are formed. However, Akahori et al. discloses providing a resin film on a semiconductor substrate and an incident surface of light to be detected so as to cover regions corresponding to regions where the photodiodes are formed ([0027]-[0029]; Fig. 2). This is done for the purpose of protecting the underlying photodiode array structure ([0028]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. with providing a resin film covering regions corresponding to regions where the photodiodes are formed on a side of the incident surface of the light to be detected, as taught by Akahori et al. so as to protect the underlying photodiode array structure.

7. Regarding claim 3, Akahori et al. discloses providing the resin film so as to cover the entire incident surface of the light to be detected (Fig. 2).

8. Regarding claim 4, Yoneta et al. discloses the semiconductor substrate is provided with an impurity region between the photodiodes adjacent to each other for separating the photodiodes from each other ([0039]).

9. Regarding claim 5, Yoneta et al. discloses a high-impurity-concentration layer of the same conductivity type as the semiconductor substrate is formed on the incident surface side of the light to be detected, in the semiconductor substrate ([0039]).

10. Regarding claim 6, Yoneta et al. discloses the following claimed elements:

- A method of producing a photodiode array, the method comprising:
  - A step of preparing a semiconductor substrate comprised of a semiconductor of a first conductivity type ([0038]);
  - A step of forming a plurality of impurity diffused layers of a second conductivity type on one surface side of the semiconductor substrate to form a plurality of photodiodes each comprised of the impurity diffused layer and the semiconductor substrate, in array ([0039]).

11. Yet, Yoneta et al. does not disclose a step of providing a resin film for transmitting light to which the photodiodes are sensitive, so as to cover at least regions corresponding to regions where the photodiodes are formed, on another surface of the semiconductor substrate. However, Akahori et al. discloses providing a resin film on a semiconductor substrate and an incident surface of light to be detected so as to cover regions corresponding to the regions where the photodiodes are formed ([0027]-[0029]; Fig. 2). This is done for the purpose of protecting the underlying photodiode array structure ([0028]).

12. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. with providing a resin film covering regions corresponding to regions where the photodiodes are formed on another side of a semiconductor substrate, as taught by Akahori et al. so as to protect the underlying photodiode array structure.

13. Regarding claim 8, Yoneta et al. discloses forming a high-impurity-concentration layer of the first conductivity type on the other surface of the semiconductor substrate ([0039]).

14. Regarding claim 9, Yoneta et al. discloses providing an impurity region of the first conductivity type between the impurity diffused layers adjacent to each other ([0039]).

15. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneta et al. (2003/0034496 A1) in view of Akahori et al. (2001/0045577 A1) as applied to claim 1 above, and further in view of Allison (U.S. 3,748,546).

16. Regarding claim 2, Yoneta et al. and Akahori et al. disclose a photodiode array but do not disclose that it contains a plurality of depressions having a predetermined depth. However, Allison discloses forming a plurality of depressions in a photodiode array on the opposite surface side to the incident surface of light to be detected, wherein each said photodiode is formed in a bottom portion of the associated depression (col 2, lines 33-45; col 3, lines 10-21; Fig. 1). The purpose of doing this is to ensure that light that enters the device also enters the space charge region, which henceforth increases the efficiency of the device (col 4, lines 9-21). Therefore, it would

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have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. and Akahori et al. with forming a plurality of depressions wherein each photodiode is formed in a bottom portion of the associated photodiode, as taught by Allison, so as to increase the efficiency of the photo-detector device.

17. Regarding claim 3, Akahori et al. discloses providing the resin film so as to cover the entire incident surface of the light to be detected (Fig. 2).

18. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneta et al. (2003/0034496 A1) in view of Akahori et al. (2001/0045577 A1) and Allison (U.S. 3,748,546).

19. Regarding claim 7, Yoneta et al. discloses the following claimed elements:

- A method of producing a photodiode array, the method comprising:
  - A step of preparing a semiconductor substrate comprised of a semiconductor of a first conductivity type;
  - A step of forming a plurality of impurity diffused layers of a second conductivity type in bottom portions of the depressions to form a plurality of photodiodes each comprised of the impurity diffused layer and the semiconductor substrate, in array.

20. Yet, Yoneta et al. does not disclose the following:

- a) A step of forming a plurality of depressions in an array on one surface side of the semiconductor substrate;

- b) A step of providing a resin film for transmitting light to which the photodiodes are sensitive, so as to cover at least regions corresponding to regions where the photodiodes are formed, on another surface of the semiconductor substrate.

21. Regarding (a), Yoneta et al. discloses a photodiode array but does not disclose that it contains a plurality of depressions having a predetermined depth. However, Allison discloses forming a plurality of depressions in a photodiode array on the opposite surface side to the incident surface of light to be detected, wherein each said photodiode is formed in a bottom portion of the associated depression (col 2, lines 33-45; col 3, lines 10-21; Fig. 1). The purpose of doing this is to ensure that light that enters the device enters the space charge region, which henceforth increases the efficiency of the device (col 4, lines 9-21). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. with forming a plurality of depressions wherein each photodiode is formed in a bottom portion of the associated photodiode, as taught by Allison, so as to increase the efficiency of the photo-detector device.

22. Regarding (b), Akahori et al. discloses providing a resin film on a semiconductor substrate and an incident surface of light to be detected so as to cover regions corresponding to the photodiodes ([0027]-[0029]; Fig. 2). This is done for the purpose of protecting the underlying photodiode array structure ([0028]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. with providing a resin film covering regions



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corresponding to regions where the photodiodes are formed on a side of the incident surface of the light to be detected, in the semiconductor substrate, as taught by Akahori, et al. so as to protect the underlying photodiode array structure.

23. Regarding claim 8, Yoneta et al. discloses forming a high-impurity-concentration layer of the first conductivity type on the other surface of the semiconductor substrate ([0039]).

24. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneta et al. (2003/0034496 A1) in view of Akahori et al. (2001/0045577 A1) as applied to claims 1 and 6 above, respectively, and further in view of Albagli et al. (2005/0072931 A1).

25. Regarding claims 10-11, Yoneta et al. and Akahori et al. disclose a scintillator panel but disclose that it is formed on the incident surface of light to be detected (Yoneta et al., [0039]). However, Albagli et al. discloses forming a scintillator panel on a side opposite to the incident light surface so as to reduce image blurring ([0025]-[0028]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Yoneta et al. and Akahori et al. with a scintillator panel opposite to the incident surface of detected light, as taught by Albagli, so as to reduce image blurring.

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**Conclusion**

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shibayama (U.S. 7,148,464 B2), Miyata et al. (U.S. 7,002,155 B2) disclose photodiode arrays.

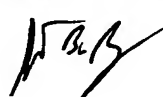
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RSP  
5/25/07

SCOTT B. GEYER  
PRIMARY EXAMINER

 5/25/07